DIGITAL INTEGRATED SYSTEM ARCHITETURES II

1. KEY INDICATORS

CFU/ECTS: 6
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2. OBJECTIVE OF THE COURSE

The objective of the course is to give the student the conceptual tools and the knowledge needed to the design of high-speed and /or low-power electronic digital circuits, emphasizing the most advanced technologies and the research topics in the field.

3. ACQUIRED ABILITIES

Design of high-speed and /or low-power digital circuits, at transistor and cell level.

4. PROGRAM OF THE COURSE

Review of Digital Systems, Evolution and diffusion of microelectronics, VLSI = architectures + circuits, Review of digital VLSI design flows .
VLSI point of view of static gates, Dynamic gates, Complex gates logic synthesis, Pass-transistor logic, NORA logic, Flip-flop, Latch, Memory cell, Delay and power consumption most significant features, Current technologic parameters. The method of Logical Effort for a high-speed logic CMOS design: a formal approach and different examples.
General concepts about layout elements, Elementary cells, Complex blocks, Notes on clock distribution (clock tree), Notes on power distribution, Elementary criteria on floorplan pad placement.
Full-custom clocking strategies : two-phase, pseudo-two-phase, true-single-phase (TSPC). Other methods clocking strategies: edge triggering; clock skew problem. Self-timed systems: micropipeline, asynchronous sequential circuits, delay insensitivity
Register file architectures; Static and dynamic memory architectures; Adder architectures: ripple, carrylookahed, carry select, Manchester, Subtractor architectures: 2's complement; Counter architectures; Multiplier architectures: serial to parallel, array, carry save array, Booth recoding, Shifter and other complex or special functions architectures, Architectures of state machines such as static and dynamic PLA's;
"Low power design": Power consumption models; Gate-level and architecture-level design methods, overview of the existing tools; Examples describing different methods

5. REFERENCES

Handouts downloadable from course website.
Weste and Eshraghian, Principles of CMOS VLSI design, I e II edition
Jan M. Rabaey: Digital Integrated Circuits: a Design Perspective, Prentice Hall

6. COURSE WEBSITE

http://vlsi.die.uniroma1.it/english/index_eng.html