LABORATORY OF SOLID STATE ELECTRONICS

1. KEY INDICATORS

CFU/ECTS: 6
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2. OBJECTIVES OF THE COURSE

The objectives of the course are essentially two: the first one is devoted to the description of the different analytical models used in simulation of nanoelectronic devices based on semiconductor materials and their numerical solution; the second one is devoted to manage independently the design of a complex device using the finite element simulator "Synopsys TCAD" (the student may choose between different devices). The course is aimed to develop the competences in the use of semiconductor device simulators and to improve the problem solving skills.

3. ACQUIRED ABILITIES

At the end of the course the students will be able to choose the best analytical model among many, depending on the simulation type and device structure. They will be able to choose the correct numerical resolution algorithm in order to optimize the computational cost. They will be able to use the simulator "Synopsys TCAD" in order to design complex devices using the correct mesh depending on the device geometry. Finally, the students will be able to properly understand the simulation results.

4. PROGRAM OF THE COURSE

PHYSICAL MODELS: Boltzmann Equation: Drift and diffusion currents, Continuity equation for currents; Drift-Diffusion Model: Equations and validity of Drift-Diffusion Model, Coupled and uncoupled numerical solution, Scharfetter-Gummel approximation, The initial solution, The boundary conditions, Generation and recombination; Hydrodynamic Model: The balance equations, Choice of variables and relationships, The collision term, Discretization of balance equations; Energy Transport Model; Monte Carlo Model: The band structure, Fermi's golden rule, the Monte Carlo method.
SIMULATION: Brief review of device simulators and introduction to the "Synopsys TCAD" suite. The student will implement, optimize and simulate a device between 4 possible different choices: 1) MOS Transistor (32 nm) in SOI Fully Depleted technology; 2) Tri-Gate Transistor (22 nm); 3) Tunnel-FET Transistor (32 nm); 4) Floating Gate memory cell (32 nm).

5. REFERENCES

Handouts distribuited in class.