Digital Integrated System Architecture Laboratory

1. KEY INDICATORS

CFU/ECTS: 6
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2. OBJECTIVES OF THE COURSE

The course is structured in a series of lectures followed by practical exercises aiming at introducing students to the different phases in the design flow of electronic circuits, with particular emphasis on digital integrated electronic systems. The objective of the course is to present and provide an applied knowledge base on modern digital system design flows, in particular through software tools and programs actually used in the industry.

3. ACQUIRED ABILITIES

Successful students will be able to write spice netlist and simulate digital circuits at transistor level; to follow a digital design flow from VHDL language, including verification by simulation, configuration of the synthesizer and synthesis, verification using logic analyzer; to write and simulate digital systems in SystemC language; they will also have acquired the basics of embedded systems programming in C language.

4. PROGRAM OF THE COURSE

CIRCUIT LEVEL DESIGN. Simulation of digital circuits at transistor level, circuit simulation (program: Ngspice) of logic gates, CMOS, PSEUDONMOS, precharge logic, buffers, memory cells.
RTL DIGITAL DESIGN. Design, simulation and synthesis of digital integrated circuits at RTL level (VHDL - programs: ModelSim - Synplify). Synthesis of a circuit on FPGA and laboratory test.
DIGITAL SYSTEM LEVEL DESIGN. Design and simulation of digital circuits at system level (SystemC language - programs: MS VisualC - SystemC library). Design of a digital subsystem at a functional level, cycle accurate executable models and verification through simulation.
SOFTWARE LEVEL DIGITAL DESING. Embedded systems programming, hardware/software interaction (C language - programs: WinAVR, vmlab). Writing code that interact with hardware, implementation of algorithms and partitioning of tasks between hardware and software.

5. REFERENCES

Houtouts distribuited in class.

6. COURSE WEBSITE

http://vlsi.die.uniroma1.it/didattica_lab_asi.html